# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-231813

(43)Date of publication of application : 16.08.2002

(51)Int.Cl. H01L 21/82
G01R 29/26
G01R 31/316
G06F 17/50

(21)Application number : 2001-026795

(22)Date of filing : 02.02.2001

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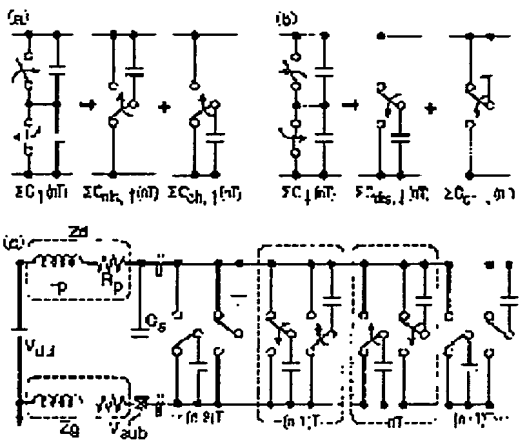
## (54) METHOD FOR ANALYZING POWER SUPPLY CURRENT WAVEFORM IN SEMICONDUCTOR INTEGRATED CIRCUIT AND ITS ANALYZING APPARATUS

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an analyzing method capable of analyzing a power supply current of a semiconductor integrated circuit including a digital circuit, with high accuracy and at high speed.

SOLUTION: In the method for analyzing the power supply current waveform in consideration of charge re-distribution process inside the digital circuit in the semiconductor integrated circuit, an analyzed digital circuit is expressed as a column of parasitic capacitances ΣCch,↑(nT), ΣCch,↓(nT) connected/charged between the power supply and a ground, which are obtained on the time series on the basis of a switching operation distributin of the logical gate circuit included in the digital circuit, and the column of parasitic capacitances is further connected with each parasitic impedance component Zd, Zg of a power supply route and a ground route and thus an analytic model is created, and by using the circuit model, the power supply current waveform of the digital circuit is obtained.



LEGAL STATUS

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|---|---|
| [Date of request for examination] | 02.02.2001 |
| [Date of sending the examiner's decision of rejection] | |
| [Kind of final disposal of application other than the examiner's decision of rejection or application converted registration] | |
| [Date of final disposal for application] | |
| [Patent number] | 3569681 |
| [Date of registration] | 25.06.2004 |
| [Number of appeal against examiner's decision of rejection] | |
| [Date of requesting appeal against examiner's decision of rejection] | |
| [Date of extinction of right] | |

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## CLAIMS

[Claim(s)]
[Claim 1] It is the approach of analyzing the power-source current wave form of a semiconductor integrated circuit including the digital circuit which consists of two or more logic-gate circuits. Said digital circuit is expressed as the parasitic capacitance train which consists of time series of the parasitic capacitance which is connected with a power source between grounds and charged based on switching operation distribution of the logic-gate circuit included in this digital circuit, and a parasitic capacitance group which is in a charge condition statically. One electrode of this parasitic capacitance train, The parasitism impedance component of one electrode of the capacity group which is in a charge condition statically, and a power-source path is connected. The analysis approach of the power-source current wave form characterized by connecting the parasitism impedance component of the electrode of another side of this parasitic capacitance train, the electrode of another side of the capacity group which is in a charge condition statically, and a ground path, generating an analytic model, and searching for the power-source current wave form of said digital circuit using this analytic model.
[Claim 2] The analysis approach of the power-source current wave form according to claim 1 characterize by generate for every logic-gate circuit group belonging to each segment at the time of divide a digital circuit into two or more segments bordering on the part into which the parasitism impedance of power-source wiring inside a digital circuit and ground wiring increase locally said parasitic capacitance train and the parasitic capacitance group which be in a charge condition statically .
[Claim 3] It is the analysis approach of the power-source current wave form according to claim 1 characterized by calculating each parasitic capacitance of said parasitic capacitance train for every predetermined time interval, and setting up the die length of this time interval according to the generating frequency distribution of the switching operation of the logic-gate circuit in the time domain where each parasitic capacitance is calculated.
[Claim 4] The die length of said time interval is the analysis approach of the power-source current wave form according to claim 3 characterized by being set up so short that the occurrence frequency of the switching operation of the logic-gate circuit in the time domain where each parasitic capacitance is calculated being large.
[Claim 5] Said parasitic capacitance charged is the analysis approach of the power-source current wave form according to claim 1 characterized by asking from the I/O capacity of the logic gate included in an analyzed digital circuit.
[Claim 6] The substrate noise analysis approach characterized by regarding it as the substrate noise which generates the voltage variation which the power-source current produced in a semiconductor integrated circuit interacts with the parasitism impedance of a power-source path and a ground path, and is generated in a semiconductor integrated circuit, and analyzing said substrate noise using the power-source current analysis approach of any one publication of claim 1 thru/or claim 5.
[Claim 7] In the design approach of the semiconductor integrated circuit which is intermingled and includes an analog circuit and a digital circuit The step which acquires a design specification, and the step which designs an analog circuit and a digital circuit based on this design specification, The step which analyzes the substrate noise which said digital circuit generates using the substrate noise analysis approach according to claim 6, The design approach of the semiconductor integrated circuit

characterized by consisting of a step which redesigns arrangement of an analog circuit, digital circuits, and these circuits, and arrangement of a guard band so that said design specification may be suited based on the analysis result of this substrate noise.

[Claim 8] It is equipment which analyzes the power-source current wave form of a semiconductor integrated circuit including the digital circuit which consists of two or more logic-gate circuits. Said digital circuit is expressed as the parasitic capacitance train which consists of time series of the parasitic capacitance which is connected with a power source between grounds and charged based on switching operation distribution of the logic-gate circuit included in this digital circuit, and a parasitic capacitance group which is in a charge condition statically. One electrode of this parasitic capacitance train, The parasitism impedance component of one electrode of the capacity group which is in a charge condition statically, and a power-source path is connected. A means to connect the parasitism impedance component of the electrode of another side of this parasitic capacitance train, the electrode of another side of the capacity group which is in a charge condition statically, and a ground path, and to generate an analytic model, Analysis equipment of the power-source current wave form characterized by consisting of a means to search for the power-source current wave form of said digital circuit using this analytic model.

[Claim 9] Analysis equipment of the power-source current wave form according to claim 8 characterize by generate for every logic-gate circuit group belonging to each segment at the time of divide a digital circuit into two or more segments bordering on the part into which the parasitism impedance of power-source wiring inside a digital circuit and ground wiring increases locally said parasitic capacitance train and the parasitic capacitance group which is in a charge condition statically .

[Claim 10] It is analysis equipment of the power-source current wave form according to claim 8 characterized by calculating each parasitic capacitance of said parasitic capacitance train for every predetermined time interval, and setting up the die length of this time interval according to the generating frequency distribution of the switching operation of the logic-gate circuit in the time domain where each parasitic capacitance is calculated.

[Claim 11] The die length of said time interval is analysis equipment of the power-source current wave form according to claim 10 characterized by being set up so short that the occurrence frequency of the switching operation of the logic-gate circuit in the time domain where each parasitic capacitance is calculated being large.

[Claim 12] Said parasitic capacitance charged is analysis equipment of the power-source current wave form according to claim 8 characterized by asking from the I/O capacity of the logic gate included in an analyzed digital circuit.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the circuit engineering using the analysis technique of the power-source current of a logical circuit and it in a large-scale semiconductor integrated circuit about the engineering of a large-scale semiconductor integrated circuit.
[0002]
[Description of the Prior Art] Scale expansion of a digital circuit and the improvement in a working speed which are carried in the interior of LSI are progressing with detailed-izing of the electronic device in a large-scale semiconductor integrated circuit (henceforth "LSI"). In recent years, the performance degradation of LSI which considered as the reason the noise generated by change of the power-source current which flows in a circuit at the time of actuation of a large-scale digital circuit, and its application system has been a remarkable problem.
[0003] The example of 1 configuration of an analog-to-digital mixed-loading semiconductor integrated circuit (henceforth "the AD mixed loading LSI") is shown in drawing 10 . Analog circuits, such as a analog-to-digital conversion circuit (ADC) which digital-value-izes the analog signal from the chip outside with high precision, and a clock generation circuit (PLL) which supplies a high-speed clock signal to an internal digital circuit, and the digital circuit which serves as a subject of signal processing, such as a microprocessor (CPU) and a digital signal processor (DSP), are loaded together on one semiconductor chip.
[0004] Via the package which carries the interior of a silicon substrate, or an LSI chip, wiring of a printed circuit board, etc., the substrate noise which a digital circuit generates leaks to an analog circuit, and is crowded with such AD mixed loading LSI, analog circuit actuation is influenced, degradation of the conversion precision of ADC and increase of fluctuation of the clock frequency of PLL are produced, and, causing degradation and malfunction of the whole chip of the engine performance of operation as a result is known.
[0005] The main generating factor of this substrate noise is for the voltage variation according to change of power-source currents, such as Ri and Ldi/dt, to arise based on a physical law, in case the power-source current of a digital circuit flows the impedance which is parasitic on the power-source path which connects an external power and an LSI chip with power-source wiring inside a circuit, and ground wiring, and a ground path.
[0006] Moreover, it interferes in the electromagnetic wave noise which LSI generates with actuation of a surrounding electronic circuitry, and it degrades the engine performance. Generating of an electromagnetic wave noise is due to the electromagnetism-interaction reflecting change of the power-source current of a digital circuit.
[0007] It is clear the yield's of these noises to depend to the variation of a power-source current strongly. Then, the analysis technique for estimating the power-source current wave form in a large-scale digital circuit block with a high speed and a sufficient precision as a design exchange technique for an LSI designer giving a performance degradation evasion measure effectively is searched for strongly.
[0008] There is the following in the analysis technique of the conventional power-source current wave form. The 1st approach is an approach of developing the whole digital circuit on transistor level, carrying out transient analysis using a circuit simulator, and searching for a power-source

current wave form. The 2nd approach is the approach of approximating by the triangular waveform to which it was presupposed that the charge-and-discharge charge of load-carrying capacity generated at the time of switching operation moves the consumed-electric-current wave of each logic gate which constitutes a digital circuit by the time amount which is switching-time extent, piling this up in the whole digital circuit, and making it into a power-source current wave form. [(K.Shimazaki, H.Tsujikawa, S.Kojima, and S.Hirano, and "LEMINGS:LSI's EMI-NoiseAnalysis with Gate Level Simulator" Proceedings of IEEE-ISQED2000) 0009]

[Problem(s) to be Solved by the Invention] There were the following problems in the above-mentioned conventional technique. Although the 1st approach can acquire a high analysis precision, since the execution time of circuit simulation becomes very large, it is not suitable for the application which needs things for which simulation by this technique is repeated and performed for every design condition, such as design optimization of the power source / ground system for the reduction in a noise, in a large-scale digital circuit. Since the 2nd approach can use a logic simulator, it can expect improvement in the speed. However, inside an actual digital circuit, migration of the high-speed charge-and-discharge charge by charge redistribution with circumference parasitic capacitance arises as an initial process of the switching operation of a logic gate, and the charge supply accompanied by the several or more times larger time constant of the switching time advances from an external power to next. Since this process is not included in the 2nd technique, reappearance of the power-source current wave form where precision is high is difficult, and is not suitable for noise analysis sensitive to time amount change of a power-source current as mentioned above.

[0010] The place which this invention is made that the above-mentioned technical problem should be solved, and is made into the purpose is to offer the analysis approach of a power-source current and analysis equipment which can enable highly precise power-source current wave form analysis in consideration of the charge redistribution process inside a digital circuit, and can be processed at a high speed. Furthermore, this invention also makes it the purpose to offer the substrate noise analysis approach of having used the highly precise and high-speed power-source current wave form analysis approach, and the low noise-ized design approach of LSI.

[0011]

[Means for Solving the Problem] The power-source current analysis approach concerning this invention is an approach of analyzing the power-source current wave form of a semiconductor integrated circuit including the digital circuit which consists of two or more logic-gate circuits. A digital circuit is expressed as the parasitic capacitance train which consists of time series of the parasitic capacitance which is connected with a power source between grounds and charged based on switching operation distribution of the logic-gate circuit included in the digital circuit, and a parasitic capacitance group which is in a charge condition statically. One electrode of the parasitic capacitance train, The parasitism impedance component of one electrode of the capacity group which is in a charge condition statically, and a power-source path is connected. And the parasitism impedance component of the electrode of another side of a parasitic capacitance train, the electrode of another side of the capacity group which is in a charge condition statically, and a ground path is connected, an analytic model is generated, and the power-source current wave form of a digital circuit is searched for using the analytic model.

[0012] in the above-mentioned power source current analysis approach , a parasitic capacitance train and the parasitic capacitance group which be in a charge condition statically may be generate for every logic gate circuit group belonging to each segment at the time of divide a digital circuit into two or more segments bordering on the part into which the parasitism impedance of power source wiring inside a digital circuit , such as a knot of the trunk/a branch line which wiring width of face be large and be different , and a knot between wiring layers , and ground wiring increase greatly locally .

[0013] In the above-mentioned power-source current analysis approach, each parasitic capacitance of a parasitic capacitance train may be calculated for every predetermined time interval, and the die length of a time interval may be set up according to the generating frequency distribution of the switching operation of the logic-gate circuit in the time domain where each parasitic capacitance is calculated.

[0014] For example, the die length of a time interval may be set up so that it may become so short

that the occurrence frequency of the switching operation of the logic-gate circuit in the time domain where each parasitic capacitance is calculated is large.
[0015] In the above-mentioned power-source current analysis approach, the parasitic capacitance charged can be calculated from the I/O capacity of the logic gate included in an analyzed digital circuit.
[0016] It considers that the substrate noise analysis approach concerning this invention is the substrate noise which generates the voltage variation which the power-source current produced in a semiconductor integrated circuit interacts with the parasitism impedance of a power-source path and a ground path, and is generated in a semiconductor integrated circuit, and it analyzes a substrate noise using the above-mentioned power-source current analysis approach.
[0017] The design approach concerning this invention consists of the step which acquires a design specification, the step which designs an analog circuit and a digital circuit based on a design specification, a step which analyze the substrate noise which a digital circuit generates using the above-mentioned substrate noise-analysis approach, and a step which redesign arrangement of an analog circuit, digital circuits, and these circuits, and arrangement of a guard band so that a design specification may suit based on the analysis result of a substrate noise in the design approach of the semiconductor integrated circuit which is intermingled and includes an analog circuit and a digital circuit.
[0018] The power-source current analysis equipment concerning this invention is equipment which analyzes the power-source current wave form of a semiconductor integrated circuit including the digital circuit which consists of two or more logic-gate circuits. A digital circuit is expressed as the parasitic capacitance train which consists of time series of the parasitic capacitance which is connected with a power source between grounds and charged based on switching operation distribution of the logic-gate circuit included in the digital circuit, and a parasitic capacitance group which is in a charge condition statically. One electrode of the parasitic capacitance train, The parasitism impedance component of one electrode of the capacity group which is in a charge condition statically, and a power-source path is connected. And it consists of a means to connect the parasitism impedance component of the electrode of another side of a parasitic capacitance train, the electrode of another side of the capacity group which is in a charge condition statically, and a ground path, and to generate an analytic model, and a means to search for the power-source current wave form of a digital circuit using the analytic model.
[0019] in above power source current analysis equipment , a parasitic capacitance train and the parasitic capacitance group which be in a charge condition statically may be generate for every logic gate circuit group belonging to each segment at the time of divide a digital circuit into two or more segments bordering on the part into which the parasitism impedance of power source wiring inside a digital circuit , such as a knot of the trunk/a branch line which wiring width of face be large and be different , and a knot between wiring layers , and ground wiring increase greatly locally .
[0020] In above power-source current analysis equipment, each parasitic capacitance of a parasitic capacitance train may be calculated for every predetermined time interval, and the die length of a time interval may be set up according to the generating frequency distribution of the switching operation of the logic-gate circuit in the time domain where each parasitic capacitance is calculated.
[0021] For example, the die length of a time interval may be set up so that it may become so short that the occurrence frequency of the switching operation of the logic-gate circuit in the time domain where parasitic capacitance is calculated is large.
[0022] In above power-source current analysis equipment, the parasitic capacitance charged can be calculated from the I/O capacity of the logic gate included in an analyzed digital circuit.
[0023]
[Embodiment of the Invention] Hereafter, the analysis approach of the power-source current wave form concerning this invention and the operation gestalt of analysis equipment are explained with reference to an attached drawing.
[0024] The concept of the analytic model of a power-source current used for the analysis approach of the power-source current wave form concerning this invention is explained to the <conceptual of power-source current analytic model> beginning.
[0025] By the analysis approach of the power-source current wave form concerning this invention, it

notes that only the charge process of the load-carrying capacity in the switching operation of each logic gate inside a digital circuit mainly contributes to formation of the power-source current in a large-scale digital circuit. A large-scale digital circuit is expressed as a parasitic capacitance train serially connected between a power source and a ground based on switching operation distribution of an internal logic-gate circuit, it considers as the current which carries out the charge and discharge of this, and a power-source current wave form is searched for. It is thought that the discharge process of the load-carrying capacity in the switching operation of each logic gate is a process which disappears according to the local short-circuit current inside a logic gate, therefore can disregard the charge charge of the load-carrying capacity by the charge process before it in [ the contribution to the power-source current of a discharge process ] approximation here.

[0026] As shown in drawing 1 , specifically, a large-scale digital circuit is treated as a set of the load parasitic capacitance to which the connection relation to power-source wiring and ground wiring is switched by the logic state. If the interior action of a large-scale digital circuit disregards the function and pays its attention only to the switching operation of an internal logic gate, it can carry out [ equal circuit ]-izing as a set of the capacity group (sigmaCst) which is parasitic on the logic gate where a condition does not change in the capacity group (sigmaC**) which is parasitic on the logic gate which starts into a certain time amount and changes, the capacity group (sigmaC**) which is parasitic on the logic gate which falls and changes, and its time amount. As shown in drawing 1 , it sets to an equal circuit, and the switching device which connects or intercepts the end of the parasitic capacitance to power-source wiring or ground wiring is prepared to each parasitic capacitance. The switching operation of the switching device which changes the connection condition of the parasitic capacitance between power-source wiring and ground wiring can express the switching operation of a logic gate appropriately.

[0027] Moreover, in drawing 1 , Cs, the power-source path, and the parasitism impedance ground system on the street are set to Zd and Zg for the parasitic capacitance which exists in the interior of the block of decoupling capacity, the well capacity in a CMOS device, etc. statically, respectively. Here, it starts and, as for transition, the output of a logic gate means the actuation in which the output of a logic gate tends to change from High to Low the actuation in which it is going to change from Low (output equal to the potential of ground wiring) to High (output equal to the potential of power-source wiring), as for falling transition.

[0028] Since the above-mentioned capacity group is distributed over high density inside the semiconductor chip with which the digital circuit is formed, the impedance of power-source wiring which connects between capacity, or ground wiring is small, and can be disregarded. Therefore, high-speed charge redistribution arises between capacity C** and C** which are parasitic on an activity logic gate, and the capacity Cst and Cs in a static condition, consequently high-speed switching operation of a logic gate is realized. Here, the capacity Cst and Cs in a static condition is functioning as ****** of a charge redistribution process. On the other hand, finally the amount of charges which should be charged is supplied from an external power. In this process, the power-source current accompanied by the time constant tau of extent shown below since it goes via the parasitism impedances Zd and Zg produces charge, consequently a substrate noise shows change slowly carried out several or more times compared with switching operation.

tau=(Zd+Zg)- (sigmaC**+sigmaC**+sigmaCst+Cs) -- (1)

[0029] (Time-sharing-izing of a parasitic capacitance train) In order to ask for time amount change of the power-source current accompanying advance of digital circuit actuation, time sharing of each capacity of a parasitic capacitance train is carried out, and a time series expression is carried out. For this reason, as shown in drawing 2 (a) - (c), the number n of the section (henceforth the "o'clock section") which carried out time sharing to the period T is introduced into the above-mentioned equal circuit. Moreover, capacity group sigmaC** (nT) which is parasitic on capacity group sigmaC** (nT) which is parasitic on the logic gate which starts and changes, and the logic gate which falls and changes is classified into capacity group sigmaCdis (nT) which discharges, respectively, and capacity sigmaCch (nT) charged, and total is taken. In addition, in drawing 2 , the notation "Cxx (nT)" to capacity Cxx expresses the capacity Cxx in the section at the n-th time.

[0030] As shown in drawing 2 (a), parasitic capacitance group sigmaC** (nT) in the standup switching operation in the section is classified into discharging capacity group sigmaCdis (nT) and

capacity group sigmaCch (nT) charged at the n-th time. As similarly shown in drawing 2 (b), parasitic capacitance group sigmaC** (nT) in the falling switching operation in the section is classified into discharging capacity group sigmaCdis (nT) and capacity group sigmaCch (nT) charged at the n-th time. In drawing 2 (a) and (b), the discharging capacity is short-circuited by switching operation, and discharges, it connects between power-source wiring and grand wiring by switching operation, and another side and the capacity charged are charged.

[0031] Amount of charges Q (nT) which moves by charge redistribution in the section at the n-th time can express supply voltage as follows as Vdd.

Q(nT)= (sigmaC** (nT) +sigmaC** (nT)), Vdd -- (2)

Among these, the discharge charge Qdis (nT) and the charge charge Qch (nT) are expressed with a degree type, respectively.

Qdis(nT)= (sigmaCdis, **(nT)+sigmaCdis, ** (nT)), Vdd -- (3)

Qch(nT)= (sigmaCch, **(nT)+sigmaCch, ** (nT)), Vdd -- (4)

[0032] The discharge charge Qdis (nT) mainly disappears according to a short-circuit current in each logic gate, and another side and the charge charge Qch (nT) are newly supplied from a power source, and are distributed and accumulated in the interior of a digital circuit. Here, the role of an external power is always supplying Qch (nT).

[0033] All the energy Ech (nT), and (=Qch(nT) and Vdd(s)) are consumed in this process, and are not related to how the electrostatic energy (= Ech/2) stored in a digital circuit dissipates in a next discharge process. Therefore, capacity group sigmaCch charged in the section (at the n-th time section) at a certain time, ** (nT), sigmaCch, and ** (nT) are connected between power-source wiring and ground wiring, and even if it separates from power-source wiring and ground wiring by carrying out short circuit discharge of such capacity in the section (at the n+1st times section) at the time of a degree, the role of an external power is not influenced. this -- a process -- the time -- the section -- every -- one after another -- repeating -- each -- ****** -- charge -- a process -- a power source -- a path -- a ground -- a system -- on the street -- parasitism -- an impedance -- an operation -- becoming settled -- a current wave -- a form -- linearity -- piling up -- things -- a digital circuit -- continuous action -- it can set -- a power source -- a current wave -- a form -- obtaining -- having . Consequently, the effectiveness of the charge redistribution in a digital circuit is incorporated by the model, and power-source current wave form analysis faithful to the charge transfer phenomenon in an actual digital circuit is attained.

[0034] The set {sigmaCch, ** (nT), sigmaCch, ** (nT)} of the parasitic capacitance charged by time series here is called a "time-sharing parasitic capacitance train." The situation of the actuation in the section is shown in (c) of drawing 2 at the n-th time of a time-sharing parasitic capacitance train. The capacity of sigmaCch and ** (n-1) (T) by which connected between power-source wiring and ground wiring, and the capacity of sigmaCch, ** (nT) and sigmaCch, and ** (nT) was connected to coincidence at the section at the time of the Tth ** (n-1) and sigmaCch, and ** (n-1) (T) connects too hastily. Moreover, the capacity of the section is in a short circuit condition at the time of others. Each capacity component can be presumed based on the network initial entry of the digital circuit after logic synthesis from the I/O capacity and the imagination wire length of the logic gate which is known beforehand, and further, if it is after a layout, high degree of accuracy can be asked more by including the parasitic capacitance of the signal wiring between logic gates extracted from layout data.

[0035] In addition, it is necessary to not necessarily set up equally the time interval T at the time of carrying out time series division (=deltat) in no time domains, and it may be changed according to the generating frequency distribution of the switching operation of a logic-gate circuit. For example, you may make it change according to the occurrence frequency of switching operation. That is, the time domain where occurrence frequency is larger may be continuously assigned the optimal so that the time interval T at the time of carrying out time sharing (=deltat) may become small, and thereby, the processing time which analysis takes can be shortened.

[0036] In addition, generally the capacity charged by each ****** is small enough compared with total of the parasitic capacitance of the whole digital circuit. Then, the parasitic capacitance group which is in a charge condition statically is approximated noting that it is equal to total of the parasitic capacitance of the whole digital circuit, it is summarized in a single capacity (equivalent to Cs of

drawing 2 (c)), and is inserted in a power-source path and ground path Uema rather than the parasitism impedance component at a digital circuit side.
[0037] (Segmentation) It is satisfactory, even if the principal component of a power-source path and the parasitism impedances Zd and Zg ground system on the street has the dominant impedance which is parasitic on wiring on the leadframe of the bonding wire and package which connect the interior and the external power of an LSI chip in a small-scale digital circuit, and a printed circuit board and it takes only these impedance components into consideration in power-source current analysis. On the other hand, it will be necessary to also take into consideration the impedance which is parasitic on metal wiring inside a chip in a large-scale digital circuit according to increase of the leading-about distance of the power-source wiring and ground wiring.
[0038] So, with this operation gestalt, the knot of the trunk/a branch line which wiring width of face is large and is different, the knot between wiring layers, etc. carry out segment division bordering on the part into which the parasitism impedance increases locally, and a time-sharing parasitic capacitance train is searched for for power-source wiring of a large-scale digital circuit, and ground wiring for every logic-gate group connected to each segment. Although it is dependent on how to take about on the layout of power-source wiring and ground wiring, as for the mode of this segment division For example, when the horizontal power-source wiring 41 of a logic-cell train and the ground wiring 43 are bundled with the perpendicular direction wiring 51 and 53 like a standard cell-based-LSI design as shown in drawing 3 (a) It is realizable by giving a definition as one segments M1 and M2 and -- every horizontal power-source wiring 41 and ground wiring 43 (every [ namely, ] logic-cell train). Each segments M1 and M2 and -- have connection relation as shown in drawing 3 (b) to a power source Vdd.
[0039] On the other hand, the parasitic capacitance group which is in a charge condition statically also about a segment is approximated noting that it is equal to total of the parasitic capacitance of the whole digital circuit inside a segment, it is summarized in a single capacity, and is inserted in a power-source path and ground path Uema rather than the parasitism impedance component at a digital circuit side.
[0040] Its attention is paid to a power-source current analytic model as mentioned above that only the charge process of the load-carrying capacity in the switching operation of each logic gate inside a digital circuit mainly contributes to formation of the power-source current in a large-scale digital circuit. It asks as a time-sharing parasitic capacitance train which expresses a large-scale digital circuit as the parasitic capacitance train serially connected and charged between a power source and a ground based on switching operation distribution of an internal logic-gate circuit as a parasitic capacitance group which is in a charge condition statically. A time-sharing parasitic capacitance train is more preferably searched for for every segment divided bordering on the part into which a parasitism impedance increases locally.
[0041] In the analytic model of the <improvement of analysis precision> above, although the charge loss by the direct short-circuit current between the power-source-grounds produced at the time of the switching operation of a logic-gate circuit is not taken into consideration, analysis precision can be raised more by taking this charge loss into consideration.
[0042] In a logic-gate circuit, a momentary power-source short circuit path smaller than the switching time (Tsw) and a ground short circuit path are formed in the interior of a circuit at the time of the switching operation. If a CMOS inverter circuit is made into an example, the charge (Qsc) (henceforth a "short circuit charge") lost here will set equally to Vth and Beta the threshold voltage and the beta value of the N type which constitutes a circuit, and P-channel MOS FET, respectively, and will be given by the degree type in approximation by setting supply voltage of a circuit to Vdd.
Qsc = {Beta/(24, Vdd)} (Vdd-2, Vth), 3, Tsw (5)
[0043] This process advances to the discharge process of the charge Qdis by switching operation and the charge process of Charge Qch, and juxtaposition, and the short circuit charge Qsc is also supplied by the charge redistribution process from surrounding ******.
[0044] However, since unlike the discharge charge Qdis an external power must be added to Charge Qch and must supply the short circuit charge Qsc and an equivalent charge, this process can be expressed equivalent by applying the capacity equivalent to the short circuit charge Qsc to charge capacity.

[0045] That is, by applying to the standup and falling capacity (the load-carrying capacity table, Table 1) of each gate circuit the capacity Csc calculated from a degree type as correction value, the effectiveness of the short circuit charge Qsc can be incorporated to a time-sharing parasitic capacitance train model, and a higher analysis precision is acquired by this.
Qsc = Csc and Vdd (6)
[0046] Generally, in the design of a digital circuit, ideally, that Beta of a standard cell is standardized by a basic value and its integral multiple extent, and since a standard cell is chosen so that it may become almost fixed, the switching time Tsw should just calculate capacity Csc as a constant.
[0047] Along with detailed-izing of MOSFET, the switching engine performance of a circuit improves, thereby, the switching time Tsw is reduced and supply voltage Vdd is low set as coincidence from reservation of device dependability. Since the short circuit charge Qsc is proportional to the square of the 1st power and supply voltage Vdd of the switching time Tsw, the error which the short circuit charge Qsc gives to a time-sharing parasitic capacitance train model becomes small with detailed-ization of MOSFET after all. Therefore, when applying this model to the power-source current analysis of a digital circuit in recent years, it is thought that it does not interfere even if short-circuit capacity is disregarded in initial approximation.
[0048] The <power-source current analysis approach of a large-scale digital circuit>, next the method of performing power-source current analysis of a large-scale digital circuit using the above-mentioned analytic model are explained. Drawing 4 is the flow chart of the analysis approach of this power-source current wave form. This analysis approach consists of five processings S1-S5.
[0049] In input process S1, the netlist of the gate level of the hardware description language (for example, Verilog HDL) format about the analyzed digital circuit used as the candidate for power-source current analysis or the netlist of the transistor level of a circuit description language (for example, SPICE) format is generated. Moreover, the test vector which described the input signal for operating an analyzed digital circuit is also generated. Moreover, in order to perform segment division every power-source wiring 41 as shown in drawing 3 , and ground wiring 43, the name of a power node and a ground node is assigned for every segment, and the connection relation between a logic gate or a circuit element, and a segment is clearly given into a netlist. In addition, when not segmenting, it is not necessary to give clearly the connection relation between a logic gate or a circuit element, and a segment into a netlist. Moreover, in order to perform analysis which reflected correctly the time delay of the logic gate inside a digital circuit of operation, it is desirable to include the information on the signal wiring delay model extracted from the layout or a signal wiring parasitic element in a netlist.
[0050] In the circuit node connection analysis processing S2, the netlist of an analyzed digital circuit is analyzed and the load-carrying capacity table to the digital circuit is generated. A load-carrying capacity table is a table which associated the load capacity value at the time of standup transition of the output node of each logic gate included in an analyzed digital circuit, the load capacity value at the time of the falling transition, and the segment to which the logic gate belongs, as shown in Table 1. For this reason, the output node of the logic gate included from a netlist in an analyzed digital circuit is extracted, and it asks for load capacity value Cch** charged in each at the time of standup switching of a logic gate, and falling switching, and Cch** from each extracted output node. Load capacity value can compute and obtain the capacity component charged at the time of a standup and falling switching from the input-capacitance component and wiring capacity component of the output capacitance currently extracted beforehand and a latter-part logic-gate group.
[Table 1] <Load-carrying capacity table>

| 出力ノード | セグメント属性 | 立ち上がり 充電負荷容量 | 立ち下り 充電負荷容量 |
|---|---|---|---|
| $N_1$ | $M_1$ | $C_{ch\uparrow,1}$ | $C_{ch\downarrow,1}$ |
| $N_2$ | $M_3$ | $C_{ch\uparrow,2}$ | $C_{ch\downarrow,2}$ |
| $N_3$ | $M_1$ | $C_{ch\uparrow,3}$ | $C_{ch\downarrow,3}$ |
| $N_4$ | $M_2$ | $C_{ch\uparrow,4}$ | $C_{ch\downarrow,4}$ |
| … | … | … | … |
| $N_n$ | $M_x$ | $C_{ch\uparrow,n}$ | $C_{ch\downarrow,n}$ |

[0051] In the switching audit-trail processing S3, the switching operating state of the output node of all the logic gates of an analyzed digital circuit to an analyzed test vector is analyzed and recorded in a time domain. Specifically, it analyzes how the switching operation of the output node of all the logic gates of an analyzed digital circuit has changed in the section at a certain time to an analyzed test vector. For this reason, to an analyzed digital circuit, using the time domain simulator corresponding to the symbolic convention of that netlist, simulation of a time domain of operation is performed using an analyzed test vector, and the switching time of day and the switching direction of a full power node are recorded. Here, switching operation starts and the switching direction shows transition and falling transition. To an analyzed test vector, as shown in Table 2, more specifically, it analyzes and records whether he has each output nodes N1 and N2, and any having fallen whether -- would have started and changed and having changed or change of state for every section at the time of predetermined.

[Table 2] <Switching audit trail>

| 出力ノード | 時区間 $T_1$ | $T_2$ | $T_3$ | … | $T_m$ |
|---|---|---|---|---|---|
| $N_1$ | ↓ | ↑ | ↑ | … | ↓ |
| $N_2$ | ↑ | ↑ | ↓ | … | ↑ |
| $N_3$ | ↓ | ↓ | ↑ | … | ↑ |
| $N_4$ | — | ↑ | ↓ | … | ↓ |
| … | ↑ | — | ↑ | … | — |
| $N_n$ | — | — | — | … | ↑ |

(** [ --- With no change of state ] -- It starts and they are transition and ** -- Falling transition)

[0052] In time-sharing parasitic capacitance train model generation processing S4, total of the load-carrying capacity charged is computed for every division section of every segment and the direction of a time-axis about each of the switching operation recorded by the above-mentioned switching audit-trail processing S3. As shown in Table 3, specifically, the time-sharing parasitic capacitance train table which asked for the total Cxy (section a corresponding segment, y: when [ x : ] it corresponds) of the load-carrying capacity charged to each segment for every ****** is generated. In addition, among Table 3, i and j are contained at Section Ty at the segment Mx and the time, start, and point out the charge parasitic capacitance of a standup switching node. The following time-sharing parasitic capacitance train tables are created for every test vector about the analyzed digital circuit of 1.

[Table 3] <Time-sharing parasitic capacitance train table>

時 間 →

| セグメント | | ←Δt→ $T_1$ | ←Δt→ $T_2$ | $T_3$ | … | $T_m$ |
|---|---|---|---|---|---|---|
| | $M_1$ | $C_{11}$ | $C_{12}$ | $C_{13}$ | … | $C_{1m}$ |
| | $M_2$ | $C_{21}$ | $C_{22}$ | $C_{23}$ | … | $C_{2m}$ |
| | $M_3$ | $C_{31}$ | $C_{32}$ | $C_{33}$ | … | $C_{3m}$ |
| | $M_4$ | $C_{41}$ | $C_{42}$ | $C_{43}$ | … | $C_{4m}$ |
| | … | … | … | … | … | … |
| | $M_n$ | $C_{n1}$ | $C_{n2}$ | $C_{n3}$ | … | $C_{nm}$ |

($C_{xy}= \Sigma C_{ch1,i} + \Sigma C_{ch1,j}$)

[0053] In a time-sharing parasitic capacitance train table, it asks for the total Cxy of the load-carrying capacity in Section Ty as follows concretely at the time of 1 to the segment Mx of 1. First, all the output nodes contained in Segment Mx are specified with reference to a load-carrying capacity table (Table 1). each specified output node -- receiving -- a switching audit trail (Table 2) -- referring to -- the time -- Section Ty -- it can set -- operating state (with [ start, and it /starts and ] no /change of state) -- checking -- each -- it asks for load charge capacity Cch** according to the operating state to an output node, i, Cch**, and j with reference to a load-carrying capacity table (Table 1). Thus, the load charge capacity according to the operating state of each output node for which it asked is totaled, and it asks for the total Cxy of load-carrying capacity.

[0054] Then, a circuit description language form generates each power-source wiring and the time-sharing parasitic capacitance train netlist subcircuit-ized to every [ which was divided for every ground wiring ] segment Mi (i= 1, 2 --). In a time-sharing parasitic capacitance train netlist, each capacity of a time-sharing parasitic capacitance train is described combining a switching device, as shown in drawing 2 (c). A switching device inserts the capacity which makes a pair between a power source and a ground, makes it charge in the section (i) at a certain time, and at the time of a degree, in the section (i+1), it operates on a time-axis so that it may be made to discharge locally.

[0055] In the power-source current analysis processing S5, to the time-sharing parasitic capacitance train netlist for which it asked as mentioned above, between a digital circuit and an external power and after [ if required, ] adding a wiring impedance component suitable between segments, a circuit simulator's transient analysis feature performs power-source current wave form analysis to the netlist.

[0056] the above -- having stated -- as -- the above -- a power source -- a current -- analysis -- an approach -- depending -- if -- a time-sharing parasitic capacitance train model -- setting -- a large-scale digital circuit -- a time-axis top -- the time -- every section -- charging -- having -- capacity -- a train -- ****** -- describing -- things -- the interior of a digital circuit -- the simulation technique which can be performed at a high speed is [ highly precise power-source current wave form analysis including a charge redistribution process ] realizable. Because of time-sharing parasitic capacitance train model generation, time domain actuation simulation only with highly precise once needs to be performed for every operated test vector about the digital circuit-ed of a hundreds of thousands to millions logic-gate scale. Although this takes time amount, once it generates a model, since only the only capacity serves as a candidate for analysis for every ****** by using this model, very high-speed simulation will become possible henceforth. Therefore, efficient-ization of the design item as which repeat activation of power-source current simulation under different conditions, such as effect evaluation of the power-source current wave form by the impedance of a power source / ground wiring system, and an optimum design of the decoupling circuit for noise yield evaluation and the reduction in a noise, electromagnetic wave yield evaluation, is required is realizable.

[0057] The functional block diagram of power-source current analysis equipment which enforces the analysis approach of the above-mentioned power-source current wave form to <power-source

current analysis equipment of large-scale digital circuit> drawing 5 is shown. Each functional block 11-15 of this equipment corresponds to each step of the above-mentioned analysis approach. The function of this equipment is realizable by performing a predetermined program in the computer system equipped with CPU.

[0058] In the input-process section 11, the netlist of the gate level of the hardware description language form about the analyzed digital circuit used as the candidate for power-source current analysis or the netlist of the transistor level of a circuit description language form is inputted. Moreover, the test vector which described the input signal for operating an analyzed digital circuit is also inputted. In order to perform segment division for every power-source wiring as shown in drawing 3 , and ground wiring, the name of a power node and a ground node is assigned for every segment, and the connection relation between a logic gate or a circuit element, and a segment is clearly given into a netlist. In addition, when not segmenting, it is not necessary to give the connection relation between a logic gate or a circuit element, and a segment into a netlist. In order to perform analysis which reflected correctly the time delay of the logic gate inside a digital circuit of operation, it is desirable to include the information on the signal wiring delay model extracted from the layout or a signal wiring parasitic element in a netlist.

[0059] In the circuit node connection analysis processing section 12, the netlist of an analyzed digital circuit is analyzed and the load-carrying capacity table (refer to Table 1) to the digital circuit is generated. A load-carrying capacity table is stored in the record means 21.

[0060] In the switching audit-trail processing section 13, the switching operating state of the output node of all the logic gates of an analyzed digital circuit to an analyzed test vector is analyzed and recorded in a time domain. Specifically, it analyzes how the switching operation of the output node of all the logic gates of an analyzed digital circuit has changed in the section at a certain time to an analyzed test vector. For this reason, to an analyzed digital circuit, the switching audit-trail processing section 13 performs simulation of a time domain of operation using an analyzed test vector, and records it on the record means 23 by making the switching time of day and the switching direction of a full power node into a switching audit trail (referring to Table 2).

[0061] In the time-sharing parasitic capacitance train model generation processing section 14, with reference to a switching audit trail, it classifies for every division section of every segment and the direction of a time-axis, total of the load-carrying capacity charged for every ****** is computed to each segment, and a time-sharing parasitic capacitance train table (refer to Table 3) is created about each of switching operation. Then, with a circuit description language form, each power-source wiring and the time-sharing parasitic capacitance train netlist which was divided for every ground wiring and which was subcircuit-ized for every segment are generated, and it records on the record means 25.

[0062] To the time-sharing parasitic capacitance train netlist for which it asked as mentioned above, between a digital circuit and an external power, if required, in the power-source current analysis processing section 15, the capacity which is in a charge condition statically, and a suitable wiring impedance component will be inserted between segments. The power-source current analysis processing section 15 has the simulator which has the transient analysis feature of a circuit, for example, a circuit simulator, and performs power-source current wave form analysis to the netlist finally obtained by this transient analysis feature.

[0063] Some applications of the analysis approach of the above-mentioned power-source current are explained below to <the application of the analysis approach of a power-source current wave form>.

[0064] (Application 1: Substrate noise analysis) The wave of the substrate noise which the shift register which is a general-purpose digital circuit generates was analyzed using the above-mentioned power-source current analysis approach. Here, it was regarded as the substrate noise which generates the voltage variation produced by flowing in the linear-resistance vessel (1 ohm) which the power-source current resulting from actuation of a shift register inserted in the power-source path and the ground path in a semiconductor integrated circuit, and analysis of a substrate noise wave was performed using the above-mentioned power-source current analysis approach.

[0065] A test circuit has the structure of connecting with the input with ten same blocks which consist of two 8-bit shift registers, and operating to juxtaposition. The total element number which a 8-bit shift register is the configuration which made 8 subordination connection of the standard D

type flip-flop (DFF) contained in the standard cell library designed with 0.6micromCMOS technique here, and is contained in a test circuit is about 10,000 pieces. Circuit simulation was performed based on the circuit netlist described on full transistor level about the exam circuit using the device parameter in 0.6micromCMOS technique (P type substrate-N type single well structure), the charge capacity value within each section was extracted about the case where a time interval is two, T=250ps and T=10ps, and the time-sharing parasitic capacitance train was created. Moreover, since it was small enough compared with the parasitic capacitance between power-source wiring of the whole test circuit, and ground wiring, the capacity value charged in each section used total of a full capacity component which is parasitic between the power source / ground wiring of this test circuit as the capacity component Cs in the static condition of functioning as ******.

[0066] The analysis result at the time of setting the parasitism impedance of power-source wiring and ground wiring only to series resistance component Rp=1 at drawing 6 is shown. In this case, the substrate noise wave shows the power-source current itself. Among drawing, from the left, it is the case where (a) full transistor level description netlist (the conventional approach), the model (this invention) of (b) T=10ps, and the model (this invention) of (c) T=250ps are used, and the substrate noise wave in case the input data of a shift register is three kinds, "00000000", "00110011", and "01010101", is shown in an upper case, the middle, and the lower berth, respectively. The analysis result by the full transistor level description netlist is made into the reference waveform. Although extent of activation inside a circuit differs by three kinds of above-mentioned input configurations, the wave which corresponded in the wave acquired by (a) well is acquired, and it is clear that the power-source current is correctly analyzed with this model. If the CPU time which the analysis of the period for 200ns took is compared, in (a), to it taking about 2500 seconds, both (b) and and (c) are 10 or less seconds, and improvement in the speed of 250 or more times is attained.

[0067] The test chip which carried the exam circuit and the substrate noise detector was made as an experiment with 0.6micromCMOS technique expressed previously. The observation wave of a substrate noise at the time of making it operate like the creation time of the time-sharing parasitic capacitance train which mentioned the exam circuit above is shown in drawing 7 . On the other hand, the simulation wave of the substrate noise at the time of including serial inductor component Lp=10nH in the parasitism impedance of power-source wiring and ground wiring is shown in drawing 8 using the time-sharing parasitic capacitance train model of T=250ps created to the exam circuit. When an activated state is changed with the number of shift register pairs which operates, respectively, the substrate noise wave of an about is also shown. As for the observation and simulation wave which were shown in drawing 7 and drawing 8 , it turns out that the relative size relation of the frequency component and amplitude is well in agreement qualitatively, and can be reproducing generating of a substrate noise with a sufficient precision with this model. In addition, a difference of the absolute value of both substrate noise amplitude is based on a damping effect until a substrate noise spreads the inside of a substrate from the point generating [ noise ] to an observation wave and it reaches a detector being included. This can be easily reproduced in analyzing this model combining the resistance mesh model of a substrate etc., and quantitive evaluation is attained.

[0068] In this example, since the P type substrate with which the test circuit is formed is connected to that ground wiring by low impedance, it is analyzing noting that the key factor of substrate noise generating is the leakage lump by the substrate of the voltage variation on ground wiring. The obtained result shows that the substrate noise is reproducible in practically sufficient precision with this substrate noise analysis technique. However, a substrate may be partially contained in the short circuit path about the discharge current of parasitic capacitance disregarded in the power-source current analysis by the time-sharing parasitic capacitance train model. By treating the substrate potential fluctuation by this current independently, a local substrate noise component can be analyzed especially still with high precision.

[0069] (Application 2: Design optimization of a low noise logical circuit) The analysis approach concerning this invention can be applied to the analysis of the power-source current wave form in the low switching noise logical circuit of patent No. 2997241, and a substrate noise, and can be utilized also for optimization of a noise reduction-ized design. Here, the low switching noise logical circuit of this patent connects a resistance element (addition resistance) between the terminals and

electrostatic capacity to which electrostatic capacity was added to at least a grand side edge child's one side the power-source side of the CMOS logical circuit which constitutes a digital circuit, and that electrostatic capacity (addition capacity) was added, and reduces the noise by the peak current by making slow ON of a logical element, and the charge and discharge at the time of OFF.
[0070] A time-sharing parasitic capacitance train model is created by this analysis approach about the digital subblock field (it consists of CMOS logical circuits) classified by addition resistance, and, specifically, the power-source current which flows addition resistance by carrying out circuit simulation of the circuit which consists of addition capacity, addition resistance, and this model is analyzed. Moreover, the power-source current of the whole digital block is acquired as total of the power-source current of a subblock. Analyzing the potential fluctuation by the power-source current of this total flowing to a power-source wiring impedance and a ground wiring impedance estimates a substrate noise. Optimization of the block division from the amount of power-source currents of each subblock and the substrate noise yield of a block is attained.
[0071] (Application 3: Electromagnetic wave noise analysis) In the tip VLSI to which large-scale and improvement in the speed went, change of a power-source current becomes very large, and fluctuation of the electromagnetic-field environment produced as a result influences a peripheral device, and causes malfunction. The loop-formation-like path of the power-source current formed on power-source wiring in VLSI acts as an antenna, and an electromagnetic wave noise is emitted by fluctuation of the power-source current which passes this. It is known that the reinforcement of an electromagnetic wave noise is proportional to the 1st power or more of the time amount variation (dI/dt) of a current. therefore, electromagnetism -- prediction of a highly precise power-source current wave form is indispensable to prediction of a noise. electromagnetism since according to the analysis approach of this invention the power-source power-source current wave form inside LSI is analyzable with high precision as shown in the previous application -- it is applicable also to prediction of a noise.
[0072] (Design optimization for a noise in the application 4:AD mixed loading LSI) In the design of the AD mixed loading LSI illustrated to drawing 10 , on the same chip, arrangement wiring is carried out and the layout block of the analog circuit and digital circuit which the design completed according to the individual respectively is unified. At this time, the circuit engine performance guaranteed according to the individual deteriorates in response to the effect of the noise at the time of digital circuit actuation about each circuit. For this reason, the real engine performance at the time of actuation of each circuit on AD mixed-loading chip is predicted, and the design technique which takes the measures against a noise so that the chip engine performance may suit a design specification is required. As the reduction technique of the effect of a noise, separation of power-source wiring between each circuit and ground wiring, installation of a decoupling circuit, insertion of the guard band of a between [ each circuit ], separation of the timing of operation on the time-axis of each circuit, the noise-proof design of an analog circuit, the low switching noise-ized design of a digital circuit, etc. are raised, for example. It is required to attain optimization of a circuit using the above noise reduction technique, performing substrate noise analysis in the AD mixed loading LSI for a low noise-ized design.
[0073] Below, the low noise-ized design flow in the AD mixed loading LSI adapting the substrate noise analysis based on this invention is explained using drawing 9 .
[0074] Before explaining the flow of drawing 9 , the library referred to at the time of the design of an analog circuit and a digital circuit is explained. Generally, in case the AD mixed loading LSI is designed, the library where the information on a designed analog circuit was registered, and the library where the information on a designed digital circuit was registered are used. Especially, speaking of the digital circuit, design datas, such as a hardware description model (netlist) of the gate level of a circuit or behavioral description level, a layout, and a test vector, are registered into the library as circuit information. In this example, in order to use the above-mentioned substrate noise analysis approach in addition to such information, about the digital circuit registered into a library, a time-sharing parasitic capacitance train model is created to the test vector for every functional actuation, and it registers with the library.
[0075] With reference to drawing 9 , the design specification of the AD mixed loading LSI is acquired first (S21).

[0076] The design of an analog circuit and a digital circuit is performed so that the design specification may be suited (S22). A circuit design selects, respectively what suits a design specification from the analog registered into the library, and a digital circuit. About an analog circuit, the case where all or some of circuits selected from the circuits registered into the library are improved and used, and the thing which designed newly and was registered so that a design specification might be suited may be used. About the design of a digital circuit, the case where the designed circuit registered into the library is used, and the thing which designed newly and was registered may be used. When a circuit is newly designed so that a design specification may be suited, it selects, after registering the information on the newly designed circuit into a library. Especially when it newly designs about a digital circuit, it is the design fault of a digital circuit, and a time-sharing parasitic capacitance train is generated to various test vectors at the time of verification of operation on the gate level about each function, and this is registered into a library.
[0077] Arrangement wiring of the analog circuit and digital circuit which were designed is carried out on the layout of the same chip as a block, respectively (S23). The noise reduction technique previously described with it is introduced. After arrangement wiring of block level, the parasitism impedance component of total of the parasitism capacity value of each block, and each power-source wiring and ground wiring is extracted from a layout. Moreover, the forecast of the impedance component which is parasitic on the package and mounting board at the time of chip mounting is prepared. Furthermore, the chip equal circuit of the whole LSI chip which combined the equal circuit expressing the layout structure on front faces of a chip, such as arrangement of each circuit or a guard band, power-source wiring, ground wiring and a well, and substrate contact arrangement, and the equal circuit of the semi-conductor substrate in which these are carried is created.
[0078] Then, the function of the whole chip and the engine performance are evaluated. For this reason, analysis of the whole chip of operation is carried out (S24). For this reason, the conventional method of analyzing the digital circuit which carried out the hardware description, and an analog circuit including a circuit description or a hardware description in analog-to-digital mixed-loading simulation is used. On the other hand, substrate noise analysis in the whole chip is carried out, and while analyzing the substrate noise which arrives at each circuit, the noise reduction-ized technique is introduced and optimized (substrate noise analysis is performed by the above-mentioned approach using the time-sharing parasitic capacitance train model registered into the library.). For this reason, an analyzed digital circuit is transposed to an above-mentioned time-sharing parasitic capacitance train model, and it connects with a static capacity equal to total of the parasitism capacity value of each block extracted previously, and the parasitism impedance of power-source wiring or ground wiring, and is made to operate as a noise generation source.
[0079] Thus, an analog circuit, a noise generation source, and the chip equal circuit generated previously are analyzed, and the performance degradation of the analog circuit by the substrate noise is evaluated. The performance evaluation of the whole chip becomes possible by making this result reflect in the analysis of the whole chip of operation.
[0080] From the above analysis result, it judges whether the function of the whole chip and the engine performance suit a design specification (S25). If it does not conform to a design specification, the design change of an analog circuit is performed so that more effective noise reduction-ization may be again obtained by the circuit design step (S22) to return and the predicted substrate noise. For example, the design change which raises the noise-proof nature of insertion of the guard band of a during [ arrangement wiring modification on block level and a block ] or an analog circuit block is performed. The above-mentioned step (S22-S25) is repeated until the result of the performance evaluation of the whole chip comes to suit a design specification. When the engine performance suits a design specification, this processing is ended and it progresses to latter design processing.
[0081] As mentioned above, in a library, it can perform in the time of an LSI design at high speed [ the substrate noise analysis to a digital circuit ], and correctly by registering the time-sharing parasitic capacitance train model beforehand as one of the design datas with circuit information, such as a netlist to a digital circuit. Thereby, optimization of the design for a noise at the time of the design of the AD mixed loading LSI can carry out easily.
[0082]
[Effect of the Invention] this invention -- a power source -- a current -- analysis -- an approach --

depending -- if -- a current -- analysis -- setting -- large-scale -- a digital circuit -- a time-axis -- a top -- the time -- the section -- every -- charging -- having -- parasitic capacitance -- a train -- and -- static -- charge -- a condition -- it is -- parasitic capacitance -- a group -- ****** -- having described -- an analytic model -- using -- things -- the highly precise power-source current wave form analysis including a charge redistribution process inside a digital circuit -- the simulation technique which can perform at a high speed -- being realizable .

[0083] Moreover, in the above-mentioned power-source current analysis approach, you may ask for every segment which divided the parasitic capacitance train and the parasitic capacitance group which is in a charge condition statically bordering on the part into which the parasitism impedance of power-source wiring and ground wiring increases locally, and, thereby, analysis precision can be improved further.

[0084] Moreover, in the above-mentioned power-source current analysis approach, the time interval at the time of searching for the time series of parasitic capacitance may be set up according to the generating frequency distribution of the switching operation of a logic-gate circuit. Thereby, improvement in the speed of analysis processing can be attained.

[0085] For example, by setting up the die length of a time interval so that it may become so short that the occurrence frequency of switching operation is large, while attaining improvement in the speed of analysis processing, a more accurate analysis result is obtained.

[0086] Moreover, in the above-mentioned power-source current analysis approach, the parasitic capacitance charged can be calculated from the I/O capacity of the logic gate included in an analyzed digital circuit, and can calculate parasitic capacitance easily.

[0087] According to the substrate noise analysis approach of this invention, in order to use the above-mentioned power-source current analysis approach, the highly precise analysis result of a substrate noise wave [ high speed ] is obtained.

[0088] According to the design approach of the semiconductor integrated circuit of this invention, since the above-mentioned substrate noise analysis approach is used, a more suitable low noise-ized design is attained.

[0089] this invention -- a power source -- a current -- analysis -- equipment -- depending -- if -- a current -- analysis -- setting -- large-scale -- a digital circuit -- a time-axis -- a top -- the time -- the section -- every -- charging -- having -- parasitic capacitance -- a train -- and -- static -- charge -- a condition -- it is -- parasitic capacitance -- a group -- ****** -- having described -- an analytic model -- using -- things -- the highly precise power-source current wave form analysis including a charge redistribution process inside a digital circuit -- the simulation technique which can perform at a high speed -- being realizable .

[0090] Moreover, in above power-source current analysis equipment, you may ask for every segment which divided the parasitic capacitance train and the parasitic capacitance group which is in a charge condition statically bordering on the part into which the parasitism impedance of power-source wiring and ground wiring increases locally, and, thereby, analysis precision can be improved further.

[0091] Moreover, in above power-source current analysis equipment, the time interval at the time of searching for the time series of parasitic capacitance may be set up according to the generating frequency distribution of the switching operation of a logic-gate circuit. Thereby, improvement in the speed of analysis processing can be attained.

[0092] For example, by setting up the die length of a time interval so that it may become so short that the occurrence frequency of switching operation is large, while attaining improvement in the speed of analysis processing, a more accurate analysis result is obtained.

[0093] Moreover, in above power-source current analysis equipment, the parasitic capacitance charged can be calculated from the I/O capacity of the logic gate included in an analyzed digital circuit, and can calculate parasitic capacitance easily.

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[Translation done.]

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing explaining the power-source current analytic model used for the power-source current analysis approach of this invention.
[Drawing 2] (a) Drawing explaining the condition of having classified the parasitic capacitance in a standup transition state to charge capacity and discharge capacity, drawing explaining the condition of having classified the parasitic capacitance in (b) falling transition state to charge capacity and discharge capacity, drawing explaining (c) time-sharing parasitic capacitance train.
[Drawing 3] (a) Drawing for explaining a segment, drawing showing the equal circuit of the parasitic capacitance train by which (b) segmentation was carried out.
[Drawing 4] The flow chart of the power-source current analysis approach concerning this invention.

[Drawing 5] The functional block diagram of power-source current analysis equipment.
[Drawing 6] Drawing having shown the wave-like analysis result of the substrate noise of the shift register using the power-source current analysis approach of this invention in the application 1 (when the parasitism impedance of power-source wiring and ground wiring is used only as a series resistance component).
[Drawing 7] Drawing having shown the observation wave of a substrate noise in the application 1.
[Drawing 8] Drawing having shown the wave-like analysis result of the substrate noise of the shift register using the power-source current analysis approach of this invention in the application 1 (when a serial inductor component is included in the parasitism impedance of power-source wiring and ground wiring).
[Drawing 9] The flow chart for the design optimization for a noise of the AD mixed loading LSI adapting the substrate noise analysis using the power-source current analysis of this invention.
[Drawing 10] Drawing explaining an example of the AD mixed loading LSI.
[Description of Notations]
11 Input Section 12 Circuit Node Connection Analysis Section 13 Switching Audit-Trail Section, 14 Time-sharing parasitic capacitance train model generation section 15 Power-source current analysis section, 21 Record means of a load-carrying capacity table 23 The record means of a switching audit trail, 25 Record means of a time-sharing parasitic capacitance train table / netlist Cch, capacity ** Started, changed and charged, Cch, capacity ** Fallen, changed and charged Zd Parasitism impedance of power-source wiring Zg Parasitism impedance of ground wiring.

[Translation done.]

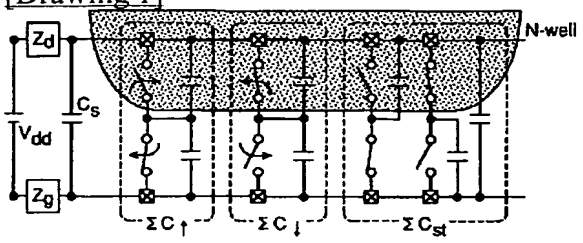
* NOTICES *



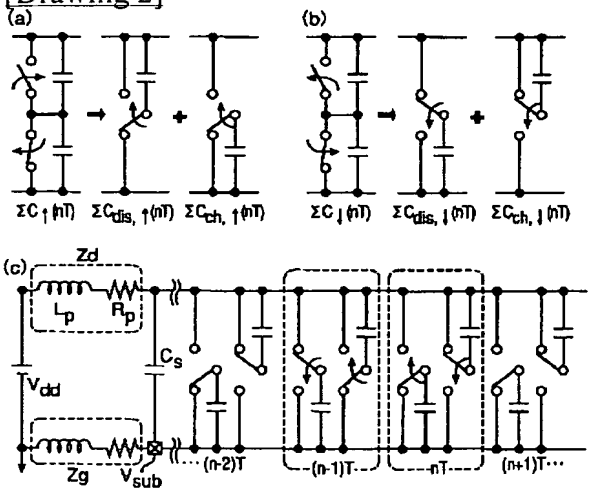
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

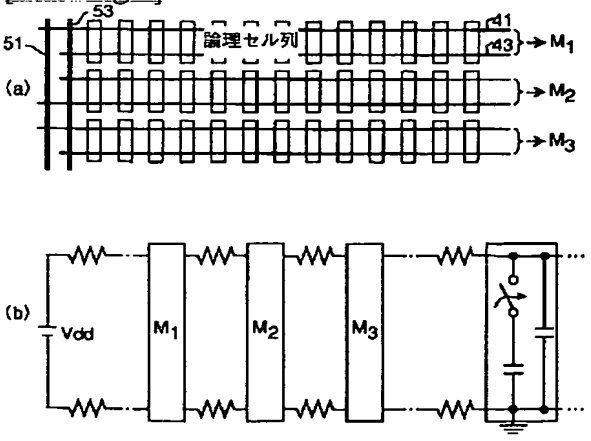
[Drawing 1]



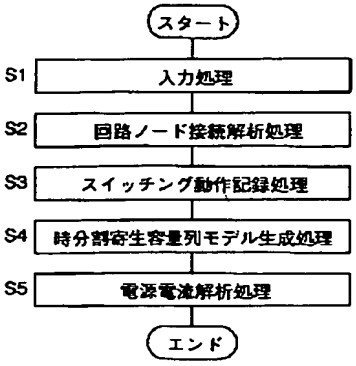

[Drawing 2]



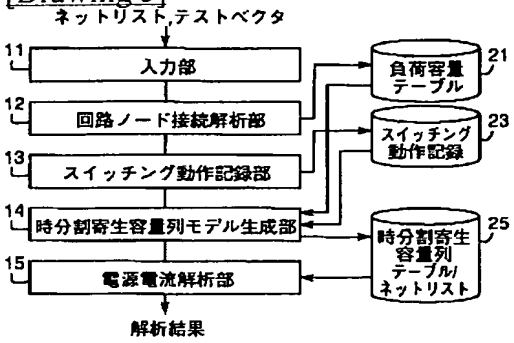

[Drawing 3]



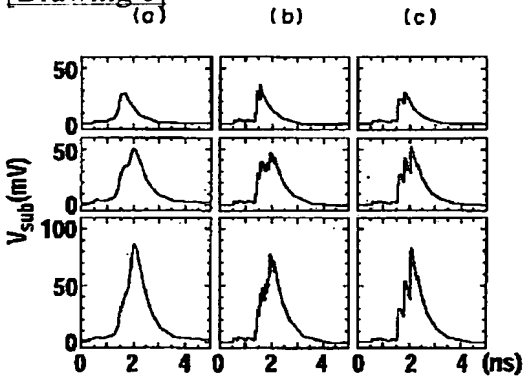

[Drawing 4]



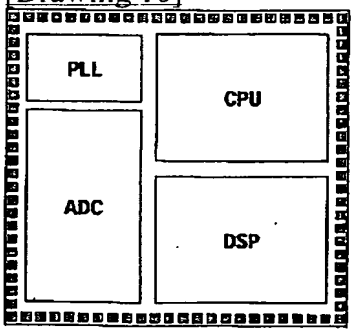

[Drawing 5]



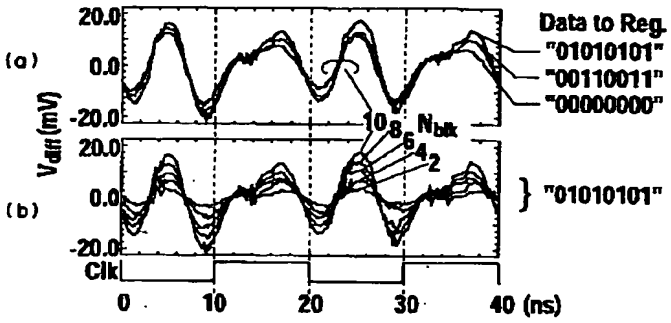

[Drawing 6]



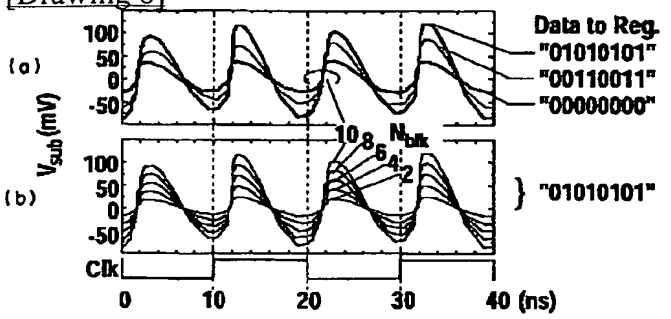

[Drawing 10]



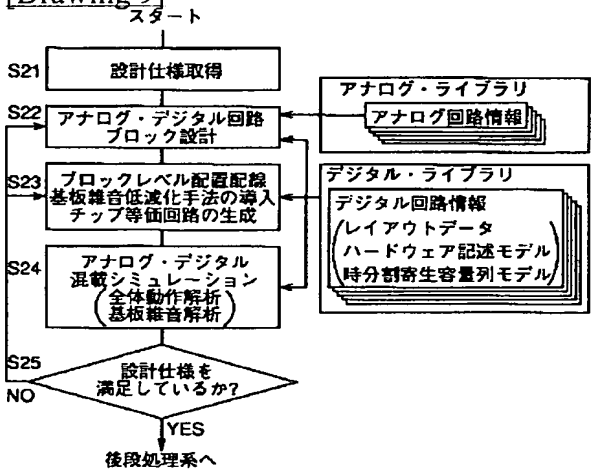

[Drawing 7]




[Drawing 8]




[Drawing 9]




[Translation done.]